

What Is Claimed Is:

1 1. A method of sharing a line bandwidth on a communication path among a
2 plurality of virtual circuits in an ATM Device, said line bandwidth equaling a line rate,
3 wherein said plurality of virtual circuits comprise a plurality of VC-types, said method
4 comprising:

5 accepting a configuration of said plurality of virtual circuits, wherein a sum of
6 allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

7 receiving a plurality of cells on said plurality of virtual circuits; and

8 scheduling for transmission said plurality of cells on said communication path
9 while enforcing a pre-specified priority with respect to said plurality of VC-types and
10 while limiting bandwidth usage by each of said plurality of virtual circuits to a
11 corresponding allocated bandwidth.

1 2. The method of claim 1, wherein said plurality of VC-types comprise constant
2 bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate -
3 non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest
4 to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that
5 order, wherein a first cell related to a lower priority VC-type is scheduled for transmission
6 only if no cells of a higher priority VC-type are ready for transmission.

1 3. The method of claim 2, wherein said plurality of VC-types further comprises
2 unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than

3 said VBR-nRT VC-type.

1 4. The method of claim 2, wherein said scheduling comprises:

2 determining cell slots in which of each of said plurality of virtual circuits is a
3 candidate for allocation according to a corresponding allocated bandwidth, wherein a first
4 virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are
5 determined to be candidates for allocation in a first cell slot on said communication path,
6 wherein said first VC-type is different from said second VC-type; and

7 allocating said first cell slot to one of said first virtual circuit and said second
8 virtual circuit having a higher priority if the virtual circuit with the higher priority has a
9 cell ready for transmission.

1 5. The method of claim 4, wherein said scheduling further comprises allocating
2 said first cell slot to one of said first virtual circuit and said second virtual circuit having
3 a lower priority if the virtual circuit with the higher priority does not have a cell ready for
4 transmission and if the virtual circuit with the lower priority has a cell ready for
5 transmission.

1 6. The method of claim 5, wherein said scheduling further comprises:

2 maintaining a VC-credit counter associated with a fourth virtual circuit comprised
3 in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of
4 cells of backlog for said fourth virtual circuit according to the corresponding allocated

5 bandwidth, but limited by a maximum number specified by a VC-type of said fourth
6 virtual circuit, wherein each cell slot on said communication path is allocated to said
7 fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

1 7. The method of claim 6, wherein said maintaining comprises:
2 initializing said VC-credit counter and a line slot credit counter associated with
3 said fourth virtual circuit to zero;
4 computing an inter-cell delay associated with said fourth virtual circuit according
5 to the corresponding allocated bandwidth; and
6 incrementing said line slot credit counter by a token value in each cell slot of said
7 communication path, wherein said token value is determined by a length of duration of
8 cell slots on said communication path;
9 incrementing said VC-credit counter by one if said line slot credit counter is equal
10 to or greater than said inter-cell delay and if said VC-credit counter is already not equal
11 to said maximum number;
12 decrementing said line slot credit counter by said inter-cell delay when said VC-
13 credit counter is incremented; and
14 decrementing said VC-credit counter by one when a cell related to said fourth
15 virtual circuit is scheduled for transmission.

1 8. The method of claim 7, further comprising:
2 computing a peak maximum slot credit and a peak intercell delay associated with

3 a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit
4 are computed according to a corresponding peak cell rate (PCR);
5 initializing a peak slot credit associated with said fifth virtual circuit to zero;
6 incrementing said peak slot credit by said token value in each cell slot, but said
7 peak slot credit being capped at said peak maximum slot credit;
8 decrementing said peak slot credit by said peak intercell delay if a cell associated
9 with said fifth virtual circuit is scheduled for transmission; and
10 scheduling for transmission a cell on said fifth virtual circuit only if said peak slot
11 credit is greater than or equal to said peak intercell delay.

1 9. The method of claim 8, wherein said fourth virtual circuit is of CBR VC-type,
2 and wherein said maximum number equals 1.

1 10. The method of claim 8, wherein said fourth virtual circuit is the same as said
2 fifth virtual circuit and is of VBR VC-type, and wherein said maximum number is
3 computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x
4 respectively represent a subtraction and a multiplication operation, PCR represents peak
5 cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of
6 said fourth virtual circuit.

1 11. The method of claim 8, wherein said ATM device comprises one of a CPE,
2 an ATM switch and a edge router.

1 12. A machine readable medium carrying one or more sequences of instructions
2 for causing an ATM device to share a line bandwidth on a communication path among
3 a plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said
4 plurality of virtual circuits comprise a plurality of VC-types, wherein execution of said
5 one or more sequences of instructions by one or more processors contained in said ATM
6 device causes said one or more processors to perform the actions of:

7 accepting a configuration of said plurality of virtual circuits, wherein a sum of
8 allocated bandwidths of said plurality of virtual circuits exceeds said line rate;
9 receiving a plurality of cells on said plurality of virtual circuits; and
10 scheduling for transmission said plurality of cells on said communication path
11 while enforcing a pre-specified priority with respect to said plurality of VC-types and
12 while limiting bandwidth usage by each of said plurality of virtual circuits to a
13 corresponding allocated bandwidth.

1 13. The machine readable medium of claim 12, wherein said plurality of VC-types
2 comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type,
3 variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority
4 comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT
5 VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled
6 for transmission only if no cells of a higher priority VC-type are ready for transmission.

1 14. The machine readable medium of claim 13, wherein said plurality of VC-types
2 further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given
3 lower priority than said VBR-nRT VC-type.

1 15. The machine readable medium of claim 13, wherein said scheduling
2 comprises:

3 determining cell slots in which of each of said plurality of virtual circuits is a
4 candidate for allocation according to a corresponding allocated bandwidth, wherein a first
5 virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are
6 determined to be candidates for allocation in a first cell slot on said communication path,
7 wherein said first VC-type is different from said second VC-type; and

8 allocating said first cell slot to one of said first virtual circuit and said second
9 virtual circuit having a higher priority if the virtual circuit with the higher priority has a
10 cell ready for transmission.

1 16. The machine readable medium of claim 15, wherein said scheduling further
2 comprises allocating said first cell slot to one of said first virtual circuit and said second
3 virtual circuit having a lower priority if the virtual circuit with the higher priority does not
4 have a cell ready for transmission and if the virtual circuit with the lower priority has a
5 cell ready for transmission.

1 17. The machine readable medium of claim 16, wherein said scheduling further

2 comprises:

3 maintaining a VC-credit counter associated with a fourth virtual circuit comprised
4 in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of
5 cells of backlog for said fourth virtual circuit according to the corresponding allocated
6 bandwidth, but limited by a maximum number specified by a VC-type of said fourth
7 virtual circuit, wherein each cell slot on said communication path is allocated to said
8 fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

1 18. The machine readable medium of claim 17, wherein said maintaining
2 comprises:

3 initializing said VC-credit counter and a line slot credit counter associated with
4 said fourth virtual circuit to zero;

5 computing an inter-cell delay associated with said fourth virtual circuit according
6 to the corresponding allocated bandwidth; and

7 incrementing said line slot credit counter by a token value in each cell slot of said
8 communication path, wherein said token value is determined by a length of duration of
9 cell slots on said communication path;

10 incrementing said VC-credit counter by one if said line slot credit counter is equal
11 to or greater than said inter-cell delay and if said VC-credit counter is already not equal
12 to said maximum number;

13 decrementing said line slot credit counter by said inter-cell delay when said VC-
14 credit counter is incremented; and

15 decrementing said VC-credit counter by one when a cell related to said fourth
16 virtual circuit is scheduled for transmission.

1 19. The machine readable medium of claim 18, further comprising:
2 computing a peak maximum slot credit and a peak intercell delay associated with
3 a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit
4 are computed according to a corresponding peak cell rate (PCR);
5 initializing a peak slot credit associated with said fifth virtual circuit to zero;
6 incrementing said peak slot credit by said token value in each cell slot, but said
7 peak slot credit being capped at said peak maximum slot credit;
8 decrementing said peak slot credit by said peak intercell delay if a cell associated
9 with said fifth virtual circuit is scheduled for transmission; and
10 scheduling for transmission a cell on said fifth virtual circuit only if said peak slot
11 credit is greater than or equal to said peak intercell delay.

1 20. The machine readable medium of claim 19, wherein said fourth virtual circuit
2 is of CBR VC-type, and wherein said maximum number equals 1.

1 21. The machine readable medium of claim 19, wherein said fourth virtual circuit
2 is the same as said fifth virtual circuit and is of VBR VC-type, and wherein said
3 maximum number is computed according to the equation $[MBS - (MBS \times SCR/PCR) -$
4 1], wherein - and \times respectively represent a subtraction and a multiplication operation,

5 PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents
6 maximum burst size of said fourth virtual circuit.

1 22. The machine readable medium of claim 19, wherein said ATM device
2 comprises one of a CPE, an ATM switch and a edge router.

1 23. An ATM device sharing a line bandwidth on a communication path among a
2 plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said plurality
3 of virtual circuits comprise a plurality of VC-types, said ATM device comprising:
4 means for accepting a configuration of said plurality of virtual circuits, wherein
5 a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;
6 means for receiving a plurality of cells on said plurality of virtual circuits; and
7 means for scheduling for transmission said plurality of cells on said
8 communication path while enforcing a pre-specified priority with respect to said plurality
9 of VC-types and while limiting bandwidth usage by each of said plurality of virtual
10 circuits to a corresponding allocated bandwidth.

1 24. The ATM device of claim 23, wherein said plurality of VC-types comprise
2 constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable
3 bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority
4 comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT
5 VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled

6 for transmission only if no cells of a higher priority VC-type are ready for transmission.

1 25. The ATM device of claim 24, wherein said plurality of VC-types further
2 comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower
3 priority than said VBR-nRT VC-type.

1 26. The ATM device of claim 24, wherein said means for scheduling is operable
2 to:

3 determine cell slots in which of each of said plurality of virtual circuits is a
4 candidate for allocation according to a corresponding allocated bandwidth, wherein a first
5 virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are
6 determined to be candidates for allocation in a first cell slot on said communication path,
7 wherein said first VC-type is different from said second VC-type; and

8 allocate said first cell slot to one of said first virtual circuit and said second virtual
9 circuit having a higher priority if the virtual circuit with the higher priority has a cell
10 ready for transmission.

1 27. The ATM device of claim 26, wherein said means for scheduling is further
2 operable to allocate said first cell slot to one of said first virtual circuit and said second
3 virtual circuit having a lower priority if the virtual circuit with the higher priority does not
4 have a cell ready for transmission and if the virtual circuit with the lower priority has a
5 cell ready for transmission.

1 28. The ATM device of claim 27, wherein said means for scheduling comprises
2 a means for maintaining a VC-credit counter associated with a fourth virtual circuit
3 comprised in said plurality of virtual circuits, wherein said VC-credit counter indicates
4 a number of cells of backlog for said fourth virtual circuit according to the corresponding
5 allocated bandwidth, but limited by a maximum number specified by a VC-type of said
6 fourth virtual circuit, wherein each cell slot on said communication path is allocated to
7 said fourth virtual circuit only if said VC-credit counter is at least greater than or equal
8 to one.

1 29. The ATM device of claim 28, wherein said means for maintaining is operable
2 to:
3 initialize said VC-credit counter and a line slot credit counter associated with said
4 fourth virtual circuit to zero;
5 compute an inter-cell delay associated with said fourth virtual circuit according to
6 the corresponding allocated bandwidth; and
7 increment said line slot credit counter by a token value in each cell slot of said
8 communication path, wherein said token value is determined by a length of duration of
9 cell slots on said communication path;
10 increment said VC-credit counter by one if said line slot credit counter is equal to
11 or greater than said inter-cell delay and if said VC-credit counter is already not equal to
12 said maximum number;

13 decrement said line slot credit counter by said inter-cell delay when said VC-credit
14 counter is incremented; and

15 decrement said VC-credit counter by one when a cell related to said fourth virtual
16 circuit is scheduled for transmission.

1 30. The ATM device of claim 29, wherein said means for maintaining is operable
2 to:

3 computing a peak maximum slot credit and a peak intercell delay associated with
4 a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit
5 are computed according to a corresponding peak cell rate (PCR);

6 initializing a peak slot credit associated with said fifth virtual circuit to zero;

7 incrementing said peak slot credit by said token value in each cell slot, but said
8 peak slot credit being capped at said peak maximum slot credit;

9 decrementing said peak slot credit by said peak intercell delay if a cell associated
10 with said fifth virtual circuit is scheduled for transmission; and

11 scheduling for transmission a cell on said fifth virtual circuit only if said peak slot
12 credit is greater than or equal to said peak intercell delay.

1 31. The ATM device of claim 30, wherein said fourth virtual circuit is of CBR
2 VC-type, and wherein said maximum number equals 1.

1 32. The ATM device of claim 30, wherein said fourth virtual circuit is the same

2 as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number
3 is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x
4 respectively represent a subtraction and a multiplication operation, PCR represents peak
5 cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of
6 said fourth virtual circuit.

1 33. The ATM device of claim 30, wherein said ATM device comprises one of a
2 CPE, a DSLAM, an ATM switch and a edge router.

1 34. An ATM device sharing a line bandwidth on a communication path among a
2 plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said plurality
3 of virtual circuits comprise a plurality of VC-types, said ATM device comprising:

4 a memory storing data representing a configuration of said plurality of virtual
5 circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits
6 exceeds said line rate;

7 an inbound interface receiving a plurality of cells on said plurality of virtual
8 circuits; and

9 a scheduler block scheduling for transmission said plurality of cells on said
10 communication path while enforcing a pre-specified priority with respect to said plurality
11 of VC-types and while limiting bandwidth usage by each of said plurality of virtual
12 circuits to a corresponding allocated bandwidth.

1 35. The ATM device of claim 34, wherein said plurality of VC-types comprise
2 constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable
3 bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority
4 comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT
5 VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled
6 for transmission only if no cells of a higher priority VC-type are ready for transmission.

1 36. The ATM device of claim 35, wherein said plurality of VC-types further
2 comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower
3 priority than said VBR-nRT VC-type.

1 37. The ATM device of claim 35, wherein said scheduler block is operable to:
2 determine cell slots in which of each of said plurality of virtual circuits is a
3 candidate for allocation according to a corresponding allocated bandwidth, wherein a first
4 virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are
5 determined to be candidates for allocation in a first cell slot on said communication path,
6 wherein said first VC-type is different from said second VC-type; and
7 allocate said first cell slot to one of said first virtual circuit and said second virtual
8 circuit having a higher priority if the virtual circuit with the higher priority has a cell
9 ready for transmission.

1 38. The ATM device of claim 37, wherein said scheduler block is further operable

2 to allocate said first cell slot to one of said first virtual circuit and said second virtual
3 circuit having a lower priority if the virtual circuit with the higher priority does not have
4 a cell ready for transmission and if the virtual circuit with the lower priority has a cell
5 ready for transmission.

1 39. The ATM device of claim 38, wherein said scheduler block is further operable
2 to maintain a VC-credit counter associated with a fourth virtual circuit comprised in said
3 plurality of virtual circuits, wherein said VC-credit counter indicates a number of cells
4 of backlog for said fourth virtual circuit according to the corresponding allocated
5 bandwidth, but limited by a maximum number specified by a VC-type of said fourth
6 virtual circuit, wherein each cell slot on said communication path is allocated to said
7 fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

1 40. The ATM device of claim 39, wherein to maintain said VC-credit, said
2 scheduler block is operable to:

3 initialize said VC-credit counter and a line slot credit counter associated with said
4 fourth virtual circuit to zero;

5 compute an inter-cell delay associated with said fourth virtual circuit according to
6 the corresponding allocated bandwidth; and

7 increment said line slot credit counter by a token value in each cell slot of said
8 communication path, wherein said token value is determined by a length of duration of
9 cell slots on said communication path;

10 increment said VC-credit counter by one if said line slot credit counter is equal to
11 or greater than said inter-cell delay and if said VC-credit counter is already not equal to
12 said maximum number;

13 decrement said line slot credit counter by said inter-cell delay when said VC-credit
14 counter is incremented; and

15 decrement said VC-credit counter by one when a cell related to said fourth virtual
16 circuit is scheduled for transmission.

1 41. The ATM device of claim 40, wherein said scheduler block is operable to:
2 compute a peak maximum slot credit and a peak intercell delay associated with a
3 fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit
4 are computed according to a corresponding peak cell rate (PCR);

5 initialize a peak slot credit associated with said fifth virtual circuit to zero;
6 increment said peak slot credit by said token value in each cell slot, but said peak
7 slot credit being capped at said peak maximum slot credit;

8 decrement said peak slot credit by said peak intercell delay if a cell associated with
9 said fifth virtual circuit is scheduled for transmission; and

10 schedule for transmission a cell on said fifth virtual circuit only if said peak slot
11 credit is greater than or equal to said peak intercell delay.

1 42. The ATM device of claim 41, wherein said fourth virtual circuit is of CBR
2 VC-type, and wherein said maximum number equals 1.

1 43. The ATM device of claim 41, wherein said fourth virtual circuit is the same
2 as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number
3 is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x
4 respectively represent a subtraction and a multiplication operation, PCR represents peak
5 cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of
6 said fourth virtual circuit.

1 44. The ATM device of claim 41, wherein said ATM device comprises one of a
2 CPE, a DSLAM, an ATM switch and a edge router.

1 45. The ATM device of claim 41, wherein said fifth virtual circuit is of UBR type.